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1. REPORT DATE (DD-MM-YYYY) 17-11-2012		2. REPORT TYPE Final Report		3. DATES COVERED (From - To) 20-May-2009 - 31-Dec-2010	
4. TITLE AND SUBTITLE Final Report: Development of Energy-Efficient Single-Electron Transistors with Oxide Nanoelectronics			5a. CONTRACT NUMBER W911NF-09-1-0258		
			5b. GRANT NUMBER		
			5c. PROGRAM ELEMENT NUMBER 8G10AZ		
6. AUTHORS Jeremy Levy			5d. PROJECT NUMBER		
			5e. TASK NUMBER		
			5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAMES AND ADDRESSES University of Pittsburgh Office of Research University of Pittsburgh Pittsburgh, PA 15213 -2303			8. PERFORMING ORGANIZATION REPORT NUMBER		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) U.S. Army Research Office P.O. Box 12211 Research Triangle Park, NC 27709-2211			10. SPONSOR/MONITOR'S ACRONYM(S) ARO		
			11. SPONSOR/MONITOR'S REPORT NUMBER(S) 56685-PH-DRP.8		
12. DISTRIBUTION AVAILABILITY STATEMENT Approved for Public Release; Distribution Unlimited					
13. SUPPLEMENTARY NOTES The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.					
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15. SUBJECT TERMS oxide nanoelectronics, single electron transistor, energy efficient					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON Jeremy Levy
a. REPORT UU	b. ABSTRACT UU	c. THIS PAGE UU			19b. TELEPHONE NUMBER 412-624-2736

## Report Title

Final Report: Development of Energy-Efficient Single-Electron Transistors with Oxide Nanoelectronics

### ABSTRACT

The principal goal of this DARPA Seedling project was to develop an oxide-based single-electron transistor and memory based on complex oxide nanostructures. The challenge was to create a device with ultra-high density and ultra-low power consumption, comparable to fundamental limits ( $\sim kT$ /gate operation) for irreversible classical computing. The specific approach involved the development of a new method for controlling the metal-insulator transition at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface. Previously, a sketch-based field-effect transistor ("SketchFET") had been demonstrated with feature sizes as small as 2 nm. Modifications of this original design were proposed in which a "floating gate" could be used to control electron flow through a device channel. The sketch-based single-electron transistor was acronym-ready ("SketchSET") and waiting to be realized.

Along the way toward the development of this device were important fundamental materials and device questions concerning the writing mechanism, its compatibility with commercial manufacturing processes, transistor fundamental speed limitations and on/off ratios, the height of energy barriers created by the writing process, the stability of written structures, and novel device building blocks such as asymmetric barriers. A great deal was learned along the way in those areas as well, with support from this project.

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**Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:**

**(a) Papers published in peer-reviewed journals (N/A for none)**

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**Number of Papers published in peer-reviewed journals:**

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**(b) Papers published in non-peer-reviewed journals (N/A for none)**

Received

Paper

**TOTAL:**

**Number of Papers published in non peer-reviewed journals:**

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**(c) Presentations**

1. "Oxide Nanoelectronics", IUMRS-ICEM2010, Soeul, Korea, August 23, 2010.
2. "Oxide Nanoelectronics", Indian Institute of Science, Bangalore, Bangalore, India, April 27, 2010.
3. "Oxide Nanoelectronics", The International School Bangalore, Bangalore, India, April 26, 2010.
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29. "Oxide Nanoelectronics On Demand", APS March Meeting, Pittsburgh, March 16, 2009.

**Number of Presentations:** 29.00

**Non Peer-Reviewed Conference Proceeding publications (other than abstracts):**

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**TOTAL:**

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<u>Received</u>	<u>Paper</u>
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**TOTAL:**

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

Received                  Paper

TOTAL:

Number of Manuscripts:

Books

Received                  Paper

TOTAL:

Patents Submitted

Patents Awarded

USPTO Patent Application 20110263116, Ultrahigh density patterning of conducting media.

Awards

Nanotech Briefs Nano50 Award  
(<http://nanotechnews.wordpress.com/2008/11/10/4th-winners-of-the-fourth-annual-nano-50%E2%84%A2-awards-2008-top-50-technologies-products-and-innovators/>)

Graduate Students

<u>NAME</u>	<u>PERCENT SUPPORTED</u>	Discipline
Cheng Cen	0.50	
Feng Bi	0.50	
Guanglei Cheng	0.50	
<b>FTE Equivalent:</b>	<b>1.50</b>	
<b>Total Number:</b>	<b>3</b>	

Names of Post Doctorates

<u>NAME</u>	<u>PERCENT SUPPORTED</u>
Shan Hu	1.00
Patrick Irvin	0.50
<b>FTE Equivalent:</b>	<b>1.50</b>
<b>Total Number:</b>	<b>2</b>

### Names of Faculty Supported

<u>NAME</u>	<u>PERCENT SUPPORTED</u>	National Academy Member
Jeremy Levy	0.09	
<b>FTE Equivalent:</b>	<b>0.09</b>	
<b>Total Number:</b>	<b>1</b>	

### Names of Under Graduate students supported

<u>NAME</u>	<u>PERCENT SUPPORTED</u>
<b>FTE Equivalent:</b>	
<b>Total Number:</b>	

### Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period: .....	0.00
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Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):.....	0.00
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The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense .....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields: .....	0.00

### Names of Personnel receiving masters degrees

NAME

**Total Number:**

### Names of personnel receiving PHDs

NAME  
Cheng Cen  
Guanglei Cheng  
**Total Number:**

2

### Names of other research staff

NAME

PERCENT SUPPORTED

**FTE Equivalent:**

**Total Number:**

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**Sub Contractors (DD882)**

**Inventions (DD882)**

**Scientific Progress**

Please see attached document.

**Technology Transfer**

# Development of Energy-Efficient Single-Electron Transistors with Oxide Nanoelectronics

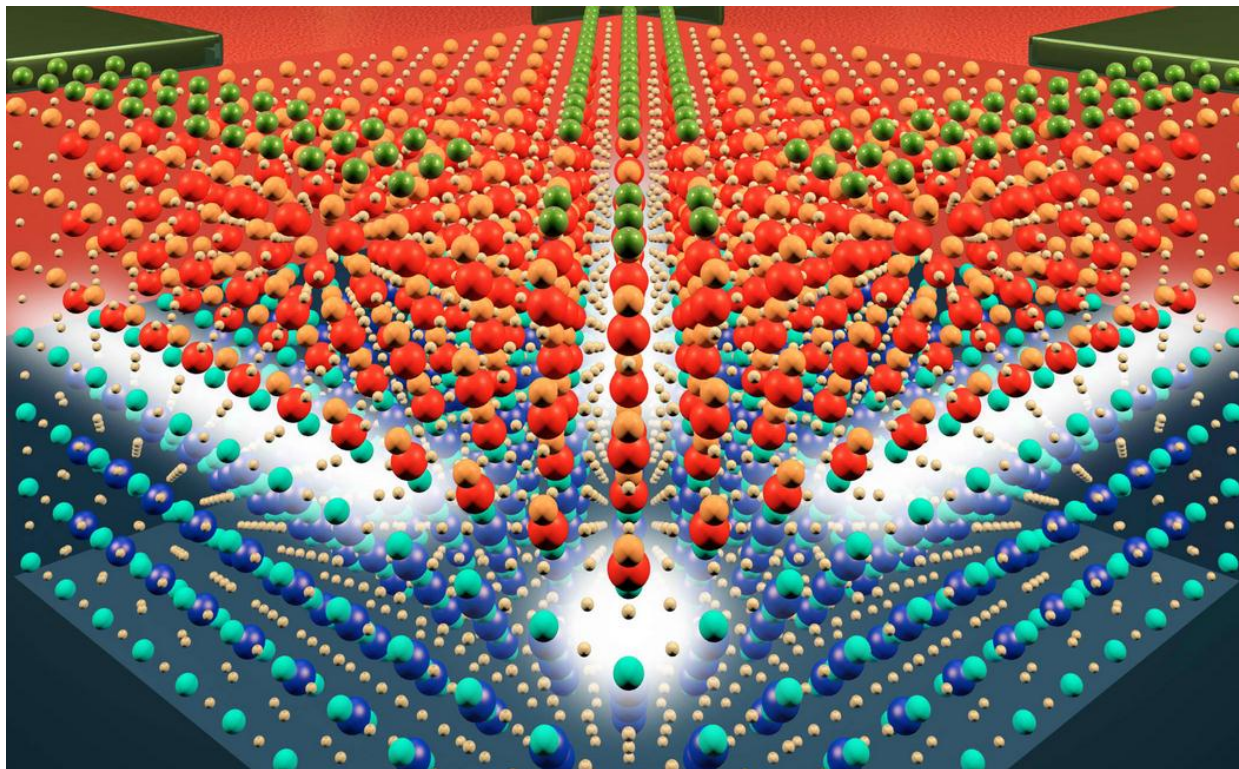
DARPA Seedling W911NF-09-10258

Jeremy Levy

*Department of Physics and Astronomy, University of Pittsburgh*

Final Report

5/1/2011



## Overview

The principal goal of this DARPA Seedling project was to develop an oxide-based single-electron transistor and memory based on complex oxide nanostructures. The challenge was to create a device with ultra-high density and ultra-low power consumption, comparable to fundamental limits ( $\sim kT/\text{gate operation}$ ) for irreversible classical computing. The specific approach involved the development of a new method for controlling the metal-insulator transition at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface. Previously, a sketch-based field-effect transistor (“SketchFET”) had been demonstrated with feature sizes as small as 2 nm. Modifications of this original design were proposed in which a “floating gate” could be used to control electron flow through a device channel. This architecture is similar to that of FLASH memory, but also of single-electron transistors. The sketch-based single-electron transistor was acronym-ready (“SketchSET”) and waiting to be realized.

Along the way toward the development of this device were important fundamental materials and device questions concerning the writing mechanism, its compatibility with commercial manufacturing processes, transistor fundamental speed limitations and on/off ratios, the height of energy barriers created by the writing process, the stability of written structures, and novel device building blocks such as asymmetric barriers. A great deal was learned along the way in those areas as well, with support from this project.

## Publications

1. G. Cheng, P. F. Siles, F. Bi, C. Cen, D. F. Bogorin, C. W. Bark, C. M. Folkman, J.-W. Park, C.-B. Eom, G. Medeiros-Ribeiro, and J. Levy, "Sketched oxide single-electron transistor," *Nature Nanotechnology*, advance online publication (2011). doi:10.1038/nnano.2011.56
2. J. W. Park, D. F. Bogorin, C. Cen, D. A. Felker, Y. Zhang, C. T. Nelson, C. W. Bark, C. M. Folkman, X. Q. Pan, M. S. Rzchowski, J. Levy, and C. B. Eom, "Creation of a two-dimensional electron gas at an oxide interface on silicon," *Nature Communications* **1**, 94 (2010).
3. P. Irvin, Y. Ma, D. F. Bogorin, C. Cen, C. W. Bark, C. M. Folkman, C.-B. Eom, and J. Levy, "Rewritable nanoscale oxide photodetector," *Nature Photonics* **4**, 849 (2010).
4. C. Cen, D. F. Bogorin, and J. Levy, "Thermal activation and quantum field emission in a sketch-based oxide nanotransistor," *Nanotechnology* **21**, 475201 (2010).
5. D. F. Bogorin, C. W. Bark, H. W. Jang, C. Cen, C. M. Folkman, C.-B. Eom, and J. Levy, "Nanoscale rectification at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface," *Appl. Phys. Lett.* **97**, 013102 (2010).
6. F. Bi, D. F. Bogorin, C. Cen, C. W. Bark, J.-W. Park, C.-B. Eom, and J. Levy, "'Water-cycle' mechanism for writing and erasing nanostructures at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface," *Appl. Phys. Lett.* **97**, 173110 (2010).

## Book chapter

1. D. F. Bogorin, P. Irvin, C. Cen, and J. Levy, "LaAlO<sub>3</sub>/SrTiO<sub>3</sub>-Based Device Concepts", <http://arxiv.org/abs/1011.5290> (2010).



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29. "Oxide Nanoelectronics On Demand", APS March Meeting, Pittsburgh, March 16, 2009.

## Doctoral Students

- Cheng Cen (Ph. D., 4/2010)
- Guanglei Cheng (Ph. D., 4/2011)
- Feng Bi

## Postdoctoral Reserchers

- Dr. Shan Hu
- Dr. Patrick Irvin

## Background

Epitaxial growth of  $\text{LaAlO}_3$  on  $\text{SrTiO}_3$  can lead to an unusual and energetically unstable charge distribution. One predicted consequence of the polar discontinuity between  $\text{LaAlO}_3$  and  $\text{SrTiO}_3$  is an interfacial insulator-to-metal transition that is dependent on the  $\text{LaAlO}_3$  thickness. This effect occurs in structures of  $\text{LaAlO}_3$  grown on  $\text{TiO}_2$ -terminated  $\text{SrTiO}_3$ . When  $\text{LaAlO}_3$  is grown with greater than a critical thickness  $d_c = 3$  unit cell (uc), the interface between  $\text{LaAlO}_3$  and  $\text{SrTiO}_3$  is found to be conducting. When the thickness of  $\text{LaAlO}_3$  is smaller than  $d_c$  the interface remains insulating. In samples grown with approximately 3 uc of  $\text{LaAlO}_3$  (normally insulating), the interface can be switched between the insulating and conducting states by applying a voltage to the back of the  $\text{SrTiO}_3$  substrate or to the top of the  $\text{LaAlO}_3$ .

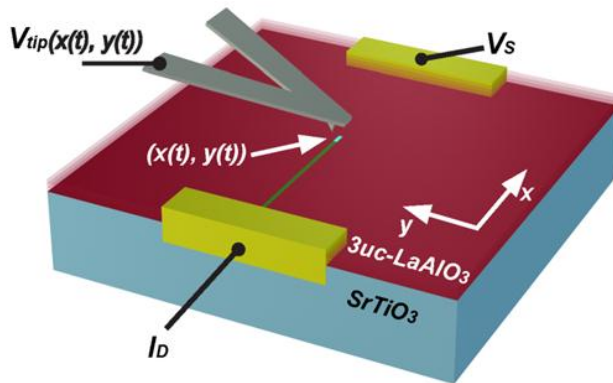


Figure 1. **Illustration of nanowire writing at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface.** Buried Au electrodes (shown in yellow) are directly contacted to the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface. The AFM tip with an applied voltage is scanned once between the two electrodes with a voltage applied  $V_{tip}(x(t), y(t))$ . Positive voltages locally switch the interface to a conducting state, while negative voltages locally restore the insulating state. Here, a conducting nanowire (shown in green) is being written. The conductance between the two electrodes is monitored by applying a small voltage bias on one of the two gold electrodes ( $V_s$ ) and reading the current at the second electrode ( $I_D$ ).

A powerful method for creating nanoscale devices at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface involves metastable charging of the top  $\text{LaAlO}_3$  surface with a conducting AFM probe (Figure 1). By locally and reversibly controlling a metal-insulator transition, the creation of both isolated and continuous conducting features has been demonstrated with length scales smaller than 2 nm. These structures can be erased and rewritten numerous times. As a result of the enormous flexibility in controlling electronic properties at near-atomic dimensions, a variety of nanoscale devices can be realized.

## Sketched Oxide Single-Electron Transistor

Devices that confine and process single electrons represent the ultimate scaling of electronics. Such control has been achieved in a variety of materials, resulting in devices with remarkable electronic, optical and spintronic properties. Oxide heterostructures formed from ultrathin layers of  $\text{LaAlO}_3$  grown on  $\text{TiO}_2$ -terminated  $\text{SrTiO}_3$ , combined with a reversible nanoscale patterning technique, provide a versatile platform for nanoscale control at the single-electron limit.

As a major accomplishment for this DARPA Seedling, we report the development of “sketched” single-electron transistors whose properties are probed through temperature-dependent transport. Shell filling from  $N=0$  up to  $N=2$  electrons by single-electron tunneling can be tuned by both bottom and side gates. Hysteresis in electron occupation is observed and attributed to ferroelectricity within the  $\text{SrTiO}_3$  tunnel barrier. These single-electron devices may find use as nanoscale hybrid piezoelectric/charge sensors, and as elemental building blocks for solid-state quantum computation and quantum simulation platforms. If device operation can be pushed up to room temperature, perhaps by substrate-induced ferroelectricity, this device could be used as a nanoscale transistor/memory.

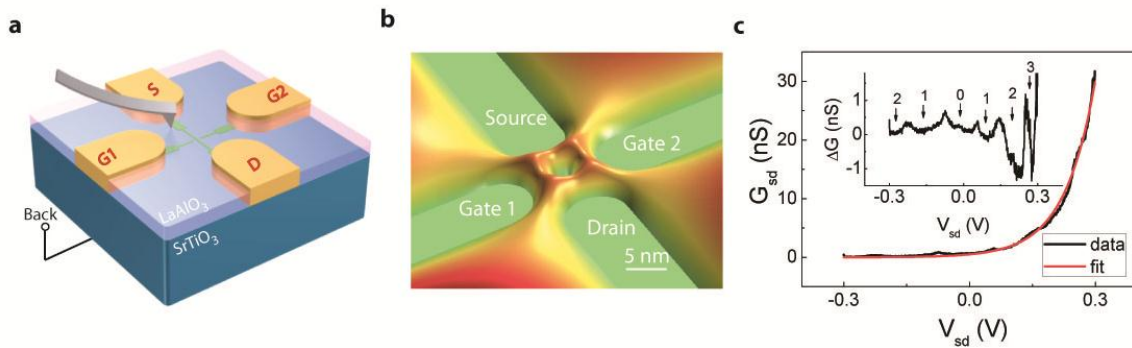
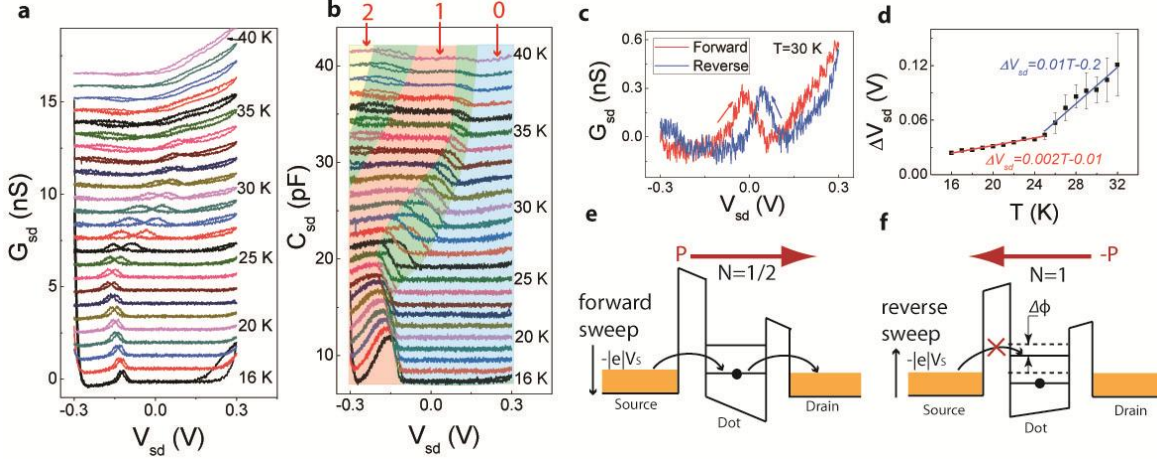


Figure 2. **SketchSET schematic and transport characteristics.** **a**, Conductive-AFM sketching of a single-electron transistor device. **b**, An energy illustration of the SketchSET device. QD tunnel barriers are created by applying a negative voltage pulse of duration  $t_b$ . The QD is formed by applying a positive voltage pulse with duration  $t_d$ . **c**, Differential conductance  $G_{sd}$  from source to drain at  $T=16$  K. The conductance is suppressed at low biases and increases rapidly above a threshold voltage  $\sim 0.2$  V. The red curve is an exponential fit to the data. The peaks in the inset are Coulomb peaks

SketchSET devices are created in a variety of ways, one of which is illustrated in Figure 2(a,b). First, two crossed nanowires are written at the  $3\text{uc-LaAlO}_3/\text{SrTiO}_3$  interface to a conducting state. The c-AFM tip is then positioned at the intersection, and an erase pulse is

applied (duration  $t_b$ , tip voltage  $V_{tip}=V_{erase}<0$ ), followed by a brief positive pulse (duration  $t_d$ ,  $V_{tip}=V_{write}>0$ ). This procedure creates an ultra-small island that behaves as a quantum dot (QD) at the intersection. The QD is surrounded by an insulating barrier and separated from the four nanowires by a narrow tunnel barrier. The center island, produced by a 10 ms write pulse, is estimated to have a diameter  $d\sim 1.5$  nm, based on a calibration of the writing process performed on the same sample. One can roughly estimate the number of electrons able to reside within the QD, based on typical two-dimensional carrier densities for nanoscale writing  $n\approx 5\times 10^{13}$  cm $^{-2}$  at the 3uc-LaAlO $_3$ /SrTiO $_3$  interface:  $N=\pi d^2 n/4\approx 1$  electron.



**Figure 3. Temperature dependent differential conductance and capacitance of Device A.** **a**, Differential conductance  $G_{sd}$  measured at temperatures ranging from 16 K (bottom black curve) to 40 K (top blue curve) in 1 K step. Curves are manually shifted by 0.6 nS for clarity. **b**, Source-drain capacitance  $C_{sd}$  measured over the same range as **a**. Curves are shifted by 1.6 pF for clarity. A sharp change in  $C_{sd}$  corresponds to a single electron tunneling event. The shadowed blue, red and yellow regions indicate electron occupation of 0, 1 and 2, respectively. The green regions indicate hysteretic regions where electron occupation in the QD changes by  $\Delta N=\pm 1$ . **c**,  $G_{sd}$  measured at  $T=30$  K for forward (red) and reverse (blue) source-drain bias sweep directions. The Coulomb peaks are shifted by ferroelectric polarization in the SrTiO $_3$ . **d**, Coulomb peak width vs. temperature. A “kink” is observed at  $T_{CI}=25$  K, coincident with a ferroelectric phase transition in the SrTiO $_3$ . **e**, Schematic band diagram showing a resonant tunneling at  $V_{sd}=0$  V in the forward sweep direction. The red arrow indicates the ferroelectric polarization direction. **f**, For the reverse sweep, the electrochemical potential of the dot is lowered by  $\Delta\phi$  so that the system is in the Coulomb blockade regime.

We focus on transport for SketchSET devices in the low-conductance regime. Figure 3(a,b) show the differential conductance  $G_{sd}$  and capacitance  $C_{sd}$  of Device A as a function of temperature (16 K to 40 K) and source-drain voltage  $V_{sd}$  (-0.3 V to 0.3 V), with all three side gates and the back gate grounded. The conductance exhibits distinct Coulomb peaks which are associated with resonant tunneling into the QD. Coinciding with these conductance peaks are abrupt changes in capacitance. Generally, increases in QD occupancy  $\Delta N=1$  are associated with roughly constant capacitance jumps  $\Delta C$ . In the blue shadowed regime in Figure 3(b), the conductance is negligible and the capacitance  $C_{sd}<\Delta C$ , is insensitive to  $V_{sd}$ . For these reasons, we infer that  $N=0$  electrons are contained in the QD in this regime.

The ferroelectric polarization has a profound influence on the resonant tunneling characteristics of the SketchSET, and is capable of switching the conductance of the source-drain channel between an “on” and “off” state (Figure 3(c)). At  $T=30$  K, when  $V_{sd}$  is swept in the forward direction, resonant tunneling is observed at  $V_{sd}=0$ , with  $G_{sd}=0.3$  nS. After sweeping  $V_{sd}$  to 0.3 V and returning to  $V_{sd}=0$ , the conductance has vanished.

The Coulomb peaks and associated capacitance jump locations exhibit hysteresis with respect to the source-drain voltage sweep direction. The conductance peak position, peak width and hysteresis magnitude vary significantly with temperature. With increasing temperature, the peak position first shifts to more negative  $V_{sd}$ , then at  $T_{CI}=25$  K it begins to increase with temperature. The width of the peak increases approximately linearly with temperature; above  $T=T_{CI}$ , the slope increases by a factor of five (Figure 3(d)).

The observed hysteresis in the Coulomb peak position is attributed to ferroelectric switching in the  $\text{SrTiO}_3$  barrier. The lattice constants of  $\text{LaAlO}_3$  and  $\text{SrTiO}_3$  are 3.789 Å and 3.905 Å respectively (3% mismatch), and the 3 uc  $\text{LaAlO}_3$  is coherently strained biaxially to match the  $\text{SrTiO}_3$  lattice constant. The profound effect of strain on thin  $\text{SrTiO}_3$  layers is well known. Field-emission experiments on  $\text{LaAlO}_3/\text{SrTiO}_3$ -based SketchFET devices show evidence of a diverging dielectric permittivity associated with structural phase transitions in the near-interface  $\text{SrTiO}_3$  region at  $T_{CI}=25$  K and  $T_{C2}=65$  K. The hysteretic behavior observed as a function of local in-plane applied electric fields is highly non-monotonic with respect to temperature, and exhibits anomalies at a known structural transition  $T_{CI}$ . This hysteresis is qualitatively distinct from hysteretic changes in polarization that have been reported for vertically gated  $\text{LaAlO}_3/\text{SrTiO}_3$  heterostructures. Hysteresis in both conduction and capacitance as a function of the back gate bias is observed for Device A; however, it is difficult to distinguish ferroelectric hysteresis from trap charging or other polarization effects in this geometry.

A remarkable feature of the SketchSET is the high sensitivity of the capacitance to changes in electron occupation in the QD. The change in capacitance ( $\sim$ pF) observed during single electron charging event at the QD is approximately three orders of magnitude too large to be accounted for solely by electrostatic effects. It is well known that  $\text{SrTiO}_3$  is a high-permittivity incipient ferroelectric with a dielectric constant that can exceed  $\epsilon \sim 10^4$  at low temperatures that is easily perturbed by structural deformation, strain and electric fields. The presence of a single bound electron at the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface is predicted to produce a large distortion of the  $\text{SrTiO}_3$  octahedra that extends far beyond the location of the charge. This structural distortion increases the polarizability of the nearby  $\text{SrTiO}_3$ , thus increasing the parasitic capacitance  $C_p$  between source and drain. The inferred  $C_{QD}$  is roughly four orders of magnitude smaller than the measured capacitance  $C_p$ .

The unique properties of this ferroelectric SketchSET provide new opportunities for combining the ultrahigh electrostatic sensitivity of SET devices with ferroelectric-derived sensitivity at the nanoscale. Because all ferroelectric materials are also piezoelectric, a natural coupling between charge and nanomechanical motion is expected for the SketchSET. Furthermore, a variety of phenomena associated with the spin degree of freedom for single-electron devices is expected to hold for these devices. By integrating oxide heterostructures with silicon, it may be possible to integrate a ferroelectric SketchSET scanning probes that are capable of measuring charge and displacement *simultaneously* at the nanoscale. The existence of a ferroelectrically programmable SET constitutes a new type of nanoscale memory architecture which could be useful for low power, ultra-high density storage, if the charging energy and ferroelectric polarization could be made to persist to room temperature. The method for creating a single SketchSET is readily replicated as a 1D or 2D array which may find use in quantum dot-based quantum computation or as a versatile solid-state ‘‘Hubbard toolbox’’ capable of exploring new artificial quantum states of matter.

## GHz switching of SketchFETs

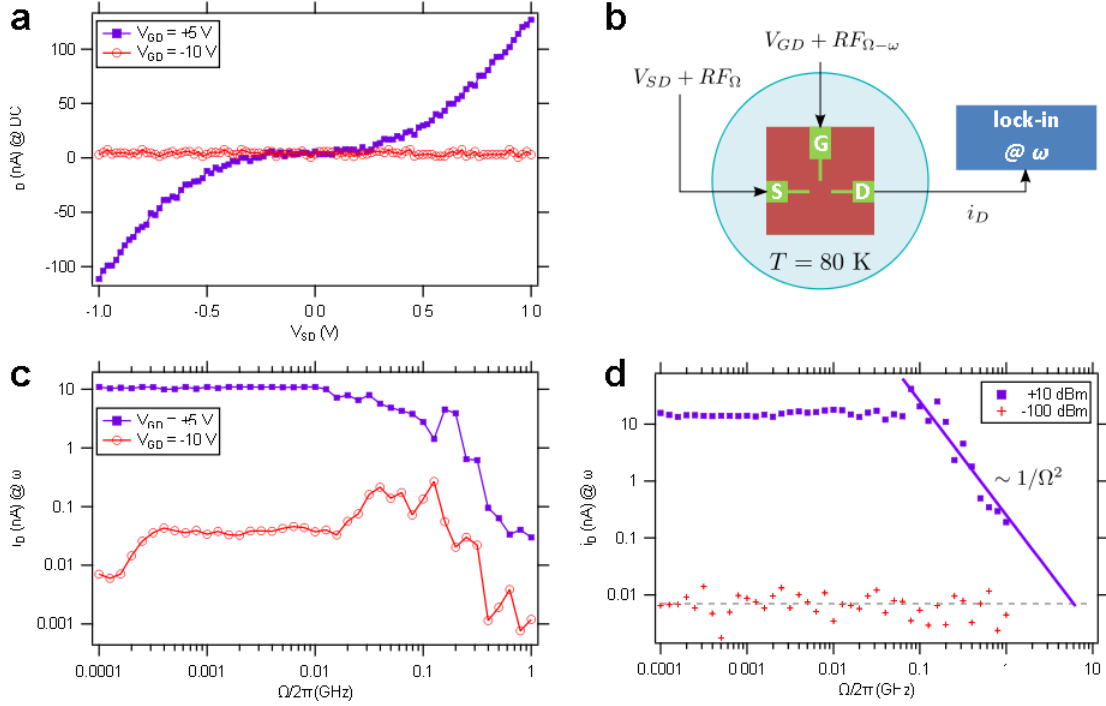


Figure 4. **Characterization of SketchFET device at GHz frequencies.** (a)  $I$ - $V$  curve of device at  $V_{GD} = +5$  V and  $-10$  V. (b) Diagram of heterodyne detection experiment. (c) Drain current measured at the difference frequency  $\omega$  as a function of RF frequency  $\Omega$ .  $V_{SD} = +1$  V and  $P_{RF} = 0$  dBm. (d) Frequency response showing cutoff frequency  $\omega_T$  at approximately 4.6 GHz.

One gauge of the performance of a transistor is its ability to modulate or amplify signals at high frequencies, as quantified by the cutoff frequency  $\omega_T$ . Characterization of the frequency dependence of the SketchFET is done using a heterodyne circuit that incorporates the SketchFET as a frequency mixer. The experimental arrangement is shown schematically (b). In addition to a DC bias that can tune the background conductance, the source electrode (ie, RF port) and gate electrode (LO port) are driven with continuous-wave RF signals of power  $P_{RF}$  at frequencies  $\Omega$  and  $\Omega - \omega$ , respectively. The current at the drain electrode (IF port) is measured on a lock-in amplifier at the difference frequency  $\omega$ . Because this is a background-free measurement, only in the case where the SketchFET operates as a frequency mixer will there be a signal of frequency  $\omega$  at the drain electrode.

In prior work to characterize the frequency response of a SketchFET,  $\omega_T$  was found to be on the order of 15 MHz and the limiting factor was mainly attributed to the resistance in the leads ( $R_S = 1$  M $\Omega$ ). By widening the leads from 12 to 100 nm we have decreased the lead resistance to 500 k $\Omega$ . Performing the heterodyne measurement described above demonstrates operation of a SketchFET at GHz frequencies (c). By extrapolating a  $1/\Omega^2$  dependence, we estimate a cutoff frequency of 4.6 GHz.



## Nanoscale phototransistors

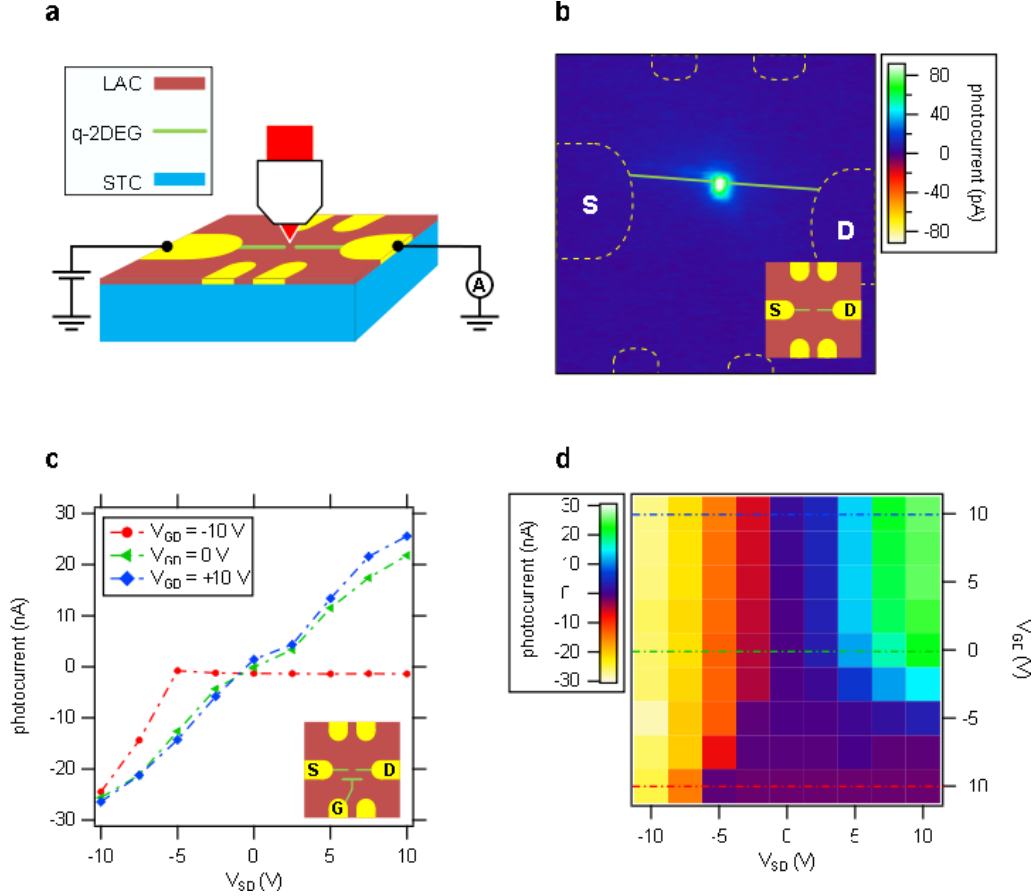


Figure 5. **Nanoscale rewritable optical photodetector.** (a) Diagram of photocurrent measurement. (b) Scanning photocurrent microscopy (SPCM) image of two-terminal device shown in inset.  $I \sim 30 \text{ kW/cm}^2$  ( $NA = 0.73$ ),  $V_{SD} = 0.1 \text{ V}$ ,  $T = 300 \text{ K}$ . (c) Photocurrent vs.  $V_{SD}$  of the three-terminal device shown in the inset.  $I \sim 20 \text{ W/cm}^2$  ( $NA = 0.13$ ),  $T = 80 \text{ K}$ . (d) Intensity map of photocurrent of three-terminal device as a function of  $V_{SD}$  and  $V_{GD}$ .

In addition to the transistors described above, one can also use AFM patterning of the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface to create rewritable, nanoscale phototransistors. Nanophotonic devices seek to generate, guide, and/or detect light using structures whose nanoscale dimensions are closely tied to their functionality. Although semiconducting nanowires, grown with tailored optoelectronic properties, have been successfully placed into devices for a variety of applications, the integration of photonic nanostructures with electronic circuitry remains one of the most challenging aspects of device development. The rewritable nanoscale phototransistors described here exhibit a remarkably high gain for their size and possess an electric field-tunable spectral response spanning the visible-to-near-infrared regime.

Optical properties of nanostructures are characterized by fixed position photocurrent measurements and spatially mapped using scanning photocurrent microscopy (SPCM) (Figure 5 (a)). The intensity of a laser source is modulated by an optical chopper at frequency  $f_R$ ; the resulting photocurrent  $i_{PC}$  is collected from a drain electrode and measured with a lock-in

amplifier at  $f_R$ . When the light overlaps with the device a sharp increase in the photocurrent is observed.

The simplest nanophotonic device consists of a nanowire with a narrow gap or junction, which can be deterministically placed with nanometer-scale accuracy. An SPCM image shows spatially-localized photocurrent detected only in the region of the junction (Figure 5(b)). The devices are erasable and reconfigurable and furthermore are not damaged by illuminating with  $\text{kW}/\text{cm}^2$  intensity: following optical characterization, devices may be erased and rewritten. The photosensitivity can be optically modulated at frequencies as high as 3.5 kHz and the response appears limited by the RC time constant of the device.

The functionality of these devices can be extended by adding an independent gate electrode using the same geometry as the previously discussed SketchFET. This bias  $V_{GD}$  can be used to modify the source-drain conductance, enabling conduction between source and drain for positive  $V_{GD}$  and inhibiting it for negative  $V_{GD}$  (Figure 5(c)). Photocurrent measured as a function of  $V_{SD}$  and  $V_{GD}$  (Figure 5(d)), exhibits a polarity that is always the same sign as the  $V_{SD}$ , irrespective of  $V_{GD}$ , indicating that there is negligible leakage current from the gate to the drain. Furthermore, the photocurrent is suppressed when both  $V_{SD}$  is positive and  $V_{GD}$  is negative, demonstrating the ability of the gate electrode to tune the photoconductivity in the source-drain channel.

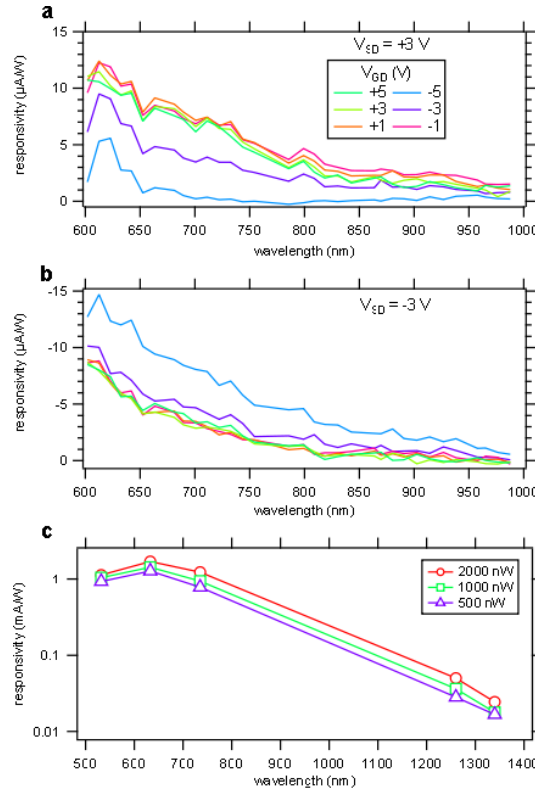


Figure 6. **Gate-controlled spectral response of phototransistor.** Fixed-position photocurrent as a function of  $\lambda$  and  $V_{GD}$  for (a)  $V_{SD} = +3$  V and (b)  $V_{SD} = -3$  V. (a) and (b):  $NA = 0.28$ ,  $T = 300$  K. (c) Responsivity of photodetector from 532 nm to 1340 nm. Lines are guides to the eye.  $V_{SD} = +2$  V,  $V_{GD} = 0$  V,  $NA = 0.13$ ,  $T = 80$  K.



To investigate the wavelength dependence of these devices, we use a variety of fixed-wavelength lasers (532 nm, 633 nm, 735 nm, 1260 nm, and 1340 nm) and also a supercontinuum white light source (600 - 1000 nm) derived from Ti:Sapphire laser. The spectral response (Figure 6) is sensitive to  $V_{SD}$  and  $V_{GD}$ . At positive  $V_{SD}$  the phototransistor response red-shifts as the gate bias is increased. A similar Stark shift is observed when sweeping the source bias. This evidence of a Stark effect, along with finite element analysis showing that the electric field is predominantly confined to the gap region, indicates that the photo-induced absorption is highly localized. Remarkably, the photosensitivity extends to 1340 nm, the longest wavelength investigated. Analysis of noise equivalent target (NET) shows a minimum NET of 11  $\text{mW}/\text{cm}^2/\sqrt{\text{Hz}}$  ( $T = 80 \text{ K}$  and  $\lambda = 735 \text{ nm}$ ).

The rewritable phototransistors presented here bring new functionality to oxide nanoelectronics. For example, existing nanowire-based molecular sensors rely on the ability to bring the analyze into contact with the sensing area of the detector. Here the roles are reversed: a nanoscale phototransistor can be placed in intimate contact with an existing molecule or biological agent. It may be possible to take advantage of the significant Stark-shifted photoresponse to improve the spatial sensitivity well beyond the diffraction limit. The ability to integrate optical and electrical components such as nanowires and transistors may lead to devices that combine in a single platform sub-wavelength optical detection with higher-level electronics-based information processing.

## Designer Potential Barriers

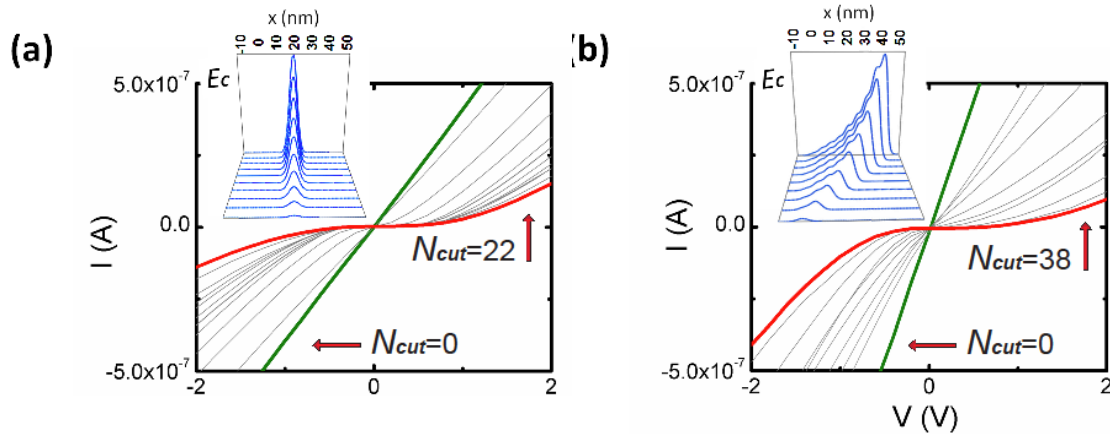


Figure 7. **Creation of designer potential barriers.** (a)  $I$ - $V$  plots for a nanowire cut at the same location multiple times with an AFM tip bias  $V_{tip} = -2 \text{ mV}$ . The green curve indicates the  $I$ - $V$  curve before the first cut. Intermediate  $I$ - $V$  curves are shown after every alternate cut. As the wire is cut, the potential barrier increases (inset) and the zero-bias conductance decreases; however, the overall  $I$ - $V$  curve remains highly reciprocal. (b)  $I$ - $V$  plots for a nanowire subject to a sequence of cuts  $N_{cut}(x)$  at nine locations spaced 5 nm apart along the nanowire. The green curve indicates  $I$ - $V$  curve before the first cut. The asymmetry in  $N_{cut}(x)$  results in a non-reciprocal  $I$ - $V$  curve.

The high degree of control over the energy landscape within the  $\text{LaAlO}_3/\text{SrTiO}_3$  2DEG allows for the development of a variety of nonlinear devices such as nanoscale junctions. The shape of the barrier can determine whether the transport is reciprocal ( $I(V) = -I(-V)$ ) or rectifying.

The controlled creation of rectifying structures is further described below. Non-reciprocal nanostructures can be created using a slightly different c-AFM manipulation. In this approach, spatial variations in the conduction-band profile are created by a precise sequence of erasure steps. In a first experiment, a conducting nanowire is created using  $V_{tip} = +10$  V. The initial  $I$ - $V$  curve (Figure 7(a), green curve) is highly linear and reciprocal. This nanowire is then cut by scanning the AFM tip across the nanowire at a speed  $v_y = 100$  nm/s using  $V_{tip} = -2$  mV at a fixed location ( $x = 20$  nm) along the length of the nanowire. This erasure process increases the conduction-band minimum  $E_c(x)$  locally by an amount that scales monotonically with the number of passes  $N_{cut}$  (Figure 7(a), inset); the resulting nanostructure exhibits a crossover from conducting to activated to tunneling behavior. Here we focus on the symmetry of the full  $I$ - $V$  curve. As  $N_{cut}$  increases, the transport becomes increasingly nonlinear; however, the  $I$ - $V$  curve remains highly reciprocal. The canvas is subsequently erased and a uniform conducting nanowire is written in a similar fashion as before ( $V_{tip} = +10$  V,  $v_x = 400$  nm/s). A similar erasure sequence is performed; however, instead of cutting the nanowire at a single  $x$  coordinate, a sequence of cuts is performed at nine adjacent  $x$  coordinates along the nanowire (separated by  $D_x = 5$  nm). The number of cuts at each location along the nanowire  $N_{cut}(x)$  increases monotonically with  $x$ , resulting in a conduction band profile  $E_c(x)$  that is asymmetric by design (Figure 7 (b), inset). The resulting  $I$ - $V$  curve for the nanostructure evolves from being highly linear and reciprocal before writing (Figure 7(b), (green curve)) to highly nonlinear and non-reciprocal (Figure 7(b), red curve).

Nanoscale control over asymmetric potential profiles at the interface between  $\text{LaAlO}_3$  and  $\text{SrTiO}_3$  can have many potential applications in nanoelectronics and spintronics. Working as straightforward diodes, these junctions can be used to create half-wave and full-wave rectifiers for AC-DC conversion or for RF detection and conversion to DC. By cascading two or more such junctions, with a third gate for tuning the density in the intermediate regime could form the basis for low-leakage transistor devices. The ability of controlling the potential along a nanowire could also be used to create wires with built-in polarizations similar to those created in heterostructures that lack inversion symmetry.

## Writing and erasing mechanism

A physical understanding of the writing and erasing mechanism is not only important for fundamental reasons but also for the development of future technologies that are based on the stability of these nanostructures. Conducting islands with densities  $>150$  Tb/in<sup>2</sup> have been demonstrated and transistors with channel lengths of 2 nm have been reported. An understanding of the physical origin of these astonishing results can help in the development of conditions that can stabilize these structures over time scales that are relevant for information storage and processing applications (i.e.,  $\sim 10$  years).

One proposed mechanism for the writing process involves the adsorption of  $\text{H}_2\text{O}$  dissociating into  $\text{OH}^-$  and  $\text{H}^+$  on the  $\text{LaAlO}_3$  surface. A conducting AFM tip provides a means to locally modify the population of charged  $\text{OH}^-$  and  $\text{H}^+$  adsorbates. This form of modulation doping locally switches the  $\text{LaAlO}_3/\text{SrTiO}_3$  interface between the insulating and conducting states. During the writing process a positively-charged AFM probe removes  $\text{OH}^-$  adsorbates, thus locally charging the top surface with the  $\text{H}^+$  ions that remain which therefore creates a conducting interface. During the erasing process, a negatively-charged AFM probe removes  $\text{H}^+$

adsorbates, restoring the interface to an insulating state. We refer to this process as a “water cycle” because it permits multiple writing and erasing without physical modification of the oxide heterostructure.

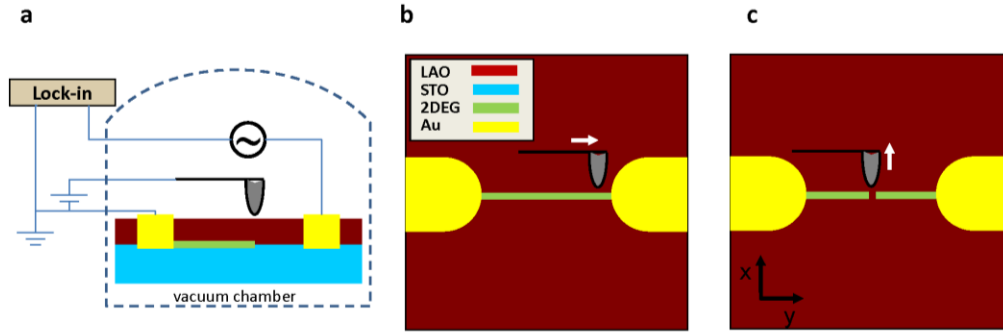


Figure 8. **Writing and erasing nanowires at 3 uc  $\text{LaAlO}_3/\text{SrTiO}_3$  interface.** (a) Side view schematic illustrating a conducting AFM probe writing a nanowire in a controlled environment. (b) Top view schematic of a writing experiment in which a nanowire is created with a positive biased tip. (c) Top view schematic of a cutting experiment in which a nanowire is locally erased with a negatively biased tip.

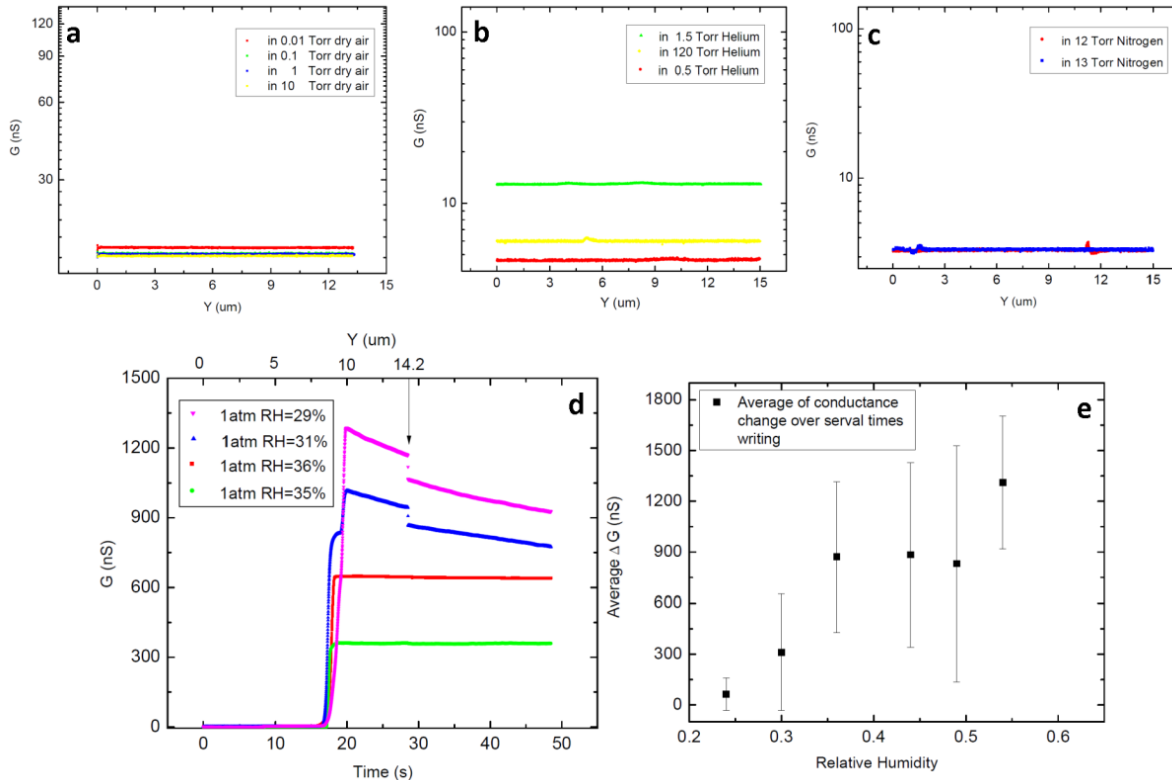


Figure 9. **Nanowire writing under various atmospheric conditions.** Writing a nanowire in (a) air, (b) helium, or (c) nitrogen environments does not result in a conducting nanowire. (d) Writing in different relative humidity (RH) level of air at 1atm. (e) Influence of RH on writing ability. All experiment are performed at  $T = 295$  K.

We have investigated the writing and erasing process under a variety of atmospheric conditions in order to constrain the physical models of the writing and erasing procedure. To perform these experiments, we use a vacuum AFM (Figure 8(a)). It is capable of operation down to  $10^{-5}$  Torr and allows for the controlled introduction of various gases. Writing and erasing experiments (Figure 8(b,c)) are performed in different atmospheres while the stability of nanostructures is monitored in real time as the ambient gaseous environment is modified. Prior to the writing, the  $\text{LaAlO}_3$  surface is alternatively raster-scanned with  $V_{tip} = \pm 10$  V to remove any adsorbates on the  $\text{LaAlO}_3$  surface and thus “initialize” the surface.

A straightforward test of the “water cycle” mechanism outlined above replaces atmospheric conditions with gas environments that lack  $\text{H}_2\text{O}$ . Figure 9(a-c) shows the results of a number of writing experiments performed using dry air (Figure 9(a)), helium (Figure 9(b)), and nitrogen (Figure 9(c)) with pressures ranging from  $10^{-2}$  -  $10^2$  Torr. Nanowires were not formed under any of these conditions. Similarly, nanowires were not formed under vacuum conditions. Next, writing experiments are performed under various conditions of relative humidity (RH). The results shown in Figure 9(d) establish that water must be present for conducting nanostructure writing.